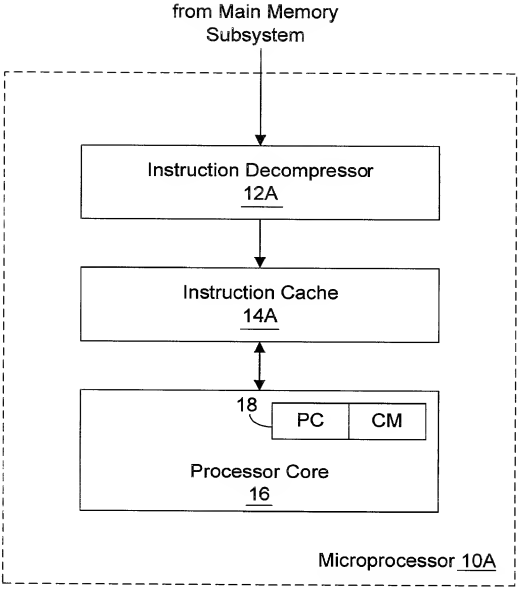

from Main Memory
Subsystem
Instruction Decompressor
12A
Instruction Cache
14A
18
PC
CM
Processor Core
16
Microprocessor 10A

FIG. 1

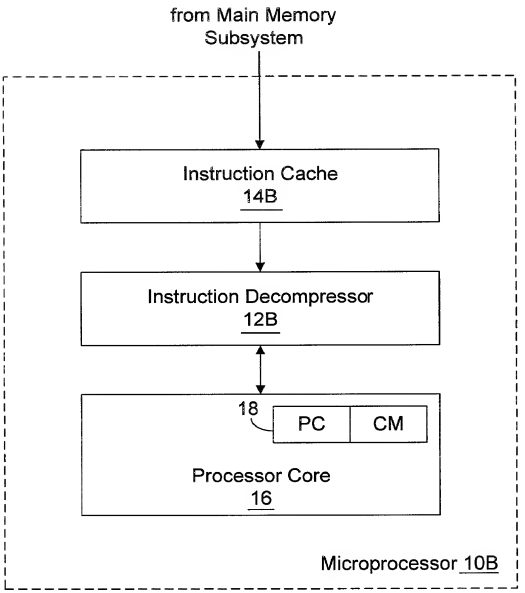
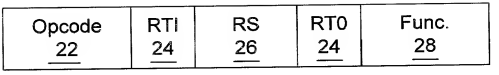
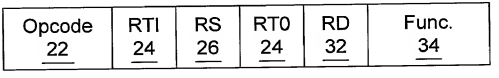

from Main Memory
Subsystem
Instruction Cache
14B
Instruction Decompressor
12B
18
PC
CM
Processor Core
16
Microprocessor 10B

FIG. 2



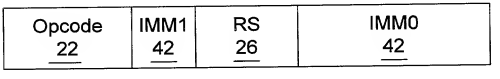
20

FIG. 3A



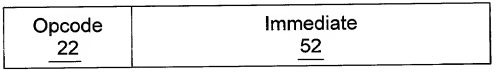
30

FIG. 3B



40

FIG. 3C



50

FIG. 3D

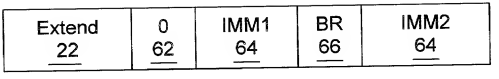


FIG. 4A

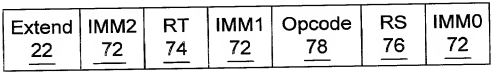


FIG. 4B

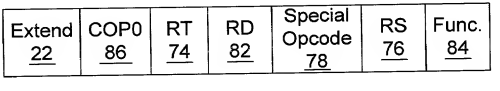


FIG. 4C

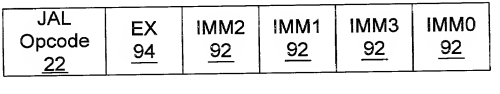


FIG. 4D

110

106 OPCODE	104 FUNC.	100 INSTRUCTION	102 OPERANDS
11	IMM5	LH	rt,rs
13	IMM5	LW	rt,xs
15	IMM5	LHU	rt,rs
17	IMM5	LW	rt,rs
18	IMM5	LB	rt,rs
19	IMM5	SH	rt,rs
1a	IMM5	SB	rt,rs
1b	IMM5	SW	rt,xs
1c	IMM5	LBU	rt,rs
1d		special	
1f	IMM5	SW	rt,rs
12	02	SLT	rs,rt
12	06	SLTU	rs,rt
12	08	MOVE	rs,xt
12	0a	SLT	rs,xt
12	0c	ADDU	rs,xt
12	0e	SLTU	rs,xt
12	10	MOVE	xs,rt
12	12	SLT	xs,rt
12	14	ADDU	xs,rt
12	16	SLTU	xs,rt
12	18	MOVE	xs,xt
12	1a	SLT	xs,xt
12	1c	ADDU	xs,xt
12	1e	SLTU	xs,xt

FIG. 5A

112

106 OPCODE	104 FUNC.	100 INSTRUCTION	102 OPERANDS
10	02	SRL	rt,imm3
10	03	SRA	rt,imm3
10	04	SLLV	rt,rs
10	06	SRLV	rt,rs
10	07	SRAV	rt,rs
10	08	JR	rs
10	09	JALR	xt,rs
10	0c	SYSCALL	imm6
10	0d	BREAK	imm6
10	10	ADD	rs,rt
10	12	SUB	rs,rt
10	13	NEG	rs,rt
10	14	AND	rs,rt
10	15	OR	rs,rt
10	16	XOR	rs,rt
10	17	NOT	rs,rt

FIG. 5B

114

106 OPCODE	104 FUNC.	100 INSTRUCTION	102 OPERANDS
12	01	ADDU	r0,rs,rt
12	03	SUBU	r0,rs,rt
12	05	ADDU	r1,rs,rt
12	07	SUBU	r1,rs,rt
12	09	ADDU	r2,rs,rt
12	0b	SUBU	r2,rs,rt
12	0d	ADDU	r3,rs,rt
12	0f	SUBU	r3,rs,rt
12	11	ADDU	r4,rs,rt
12	13	SUBU	r4,rs,rt
12	15	ADDU	r5,rs,rt
12	17	SUBU	r5,rs,rt
12	19	ADDU	r6,rs,rt
12	1b	SUBU	r6,rs,rt
12	1d	ADDU	r7,rs,rt
12	1f	SUBU	r7,rs,rt
16	imm	SLL	rd,rt,imm

FIG. 5C

116

106 OPCODE	100 INSTRUCTION	102 OPERANDS
00	BEQZ	xs,simm8
01	BNEZ	xs,simm8
04	BEQZ	rs,simm8
05	BNEZ	rs,simm8
08	MOVEI	rs,imm8
09	ADDIU	rs,simm8
0a	SLTI	rs,imm8
0b	SLTIU	rs,imm8
0c	ANDI	rs,imm8
0e	CMPI	rs,imm8

FIG. 5D

118

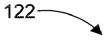
106 OPCODE	100 INSTRUCTION	102 OPERANDS
02	BR	simm11
0f	extend	imm11

FIG. 5E

120

108 OPCODE	100 INSTRUCTION	102 OPERANDS
04	BEQ	rs,rt,simm12
05	BNE	rs,rt,simm12
06	BLEZ	rs,simm12
07	BGTZ	rs,simm12
08	ADDI	rt,rs,simm12
09	ADDIU	rt,rs,simm12
0a	SLTI	rt,rs,simm12
0b	SLTIU	rt,rs,simm12
0c	ANDI	rt,rs,simm12
0d	ORI	rt,rs,simm12
0e	XORI	rt,rs,simm12
0f	LUI	rt,simm12
10	LB	rt,rs,simm12
11	LH	rt,rs,simm12
12	LWL	rt,rs,simm12
13	LW	rt,rs,simm12
14	LBU	rt,rs,simm12
15	LHU	rt,rs,simm12
16	LWR	rt,rs,simm12
18	SB	rt,rs,simm12
19	SH	rt,rs,simm12
1a	SWL	rt,rs,simm12
1b	SW	rt,rs,simm12
1e	SWR	rt,rs,simm12

FIG. 6A



109 RT	100 INSTRUCTION	102 OPERANDS
00	BLTZ	rs,simm12
01	BGEZ	rs,simm12
02	BLTZL	rs,simm12
03	BGEZL	rs,simm12
08	TGEI	rs,simm12
09	TGEIU	rs,simm12
0a	TLTI	rs,simm12
0b	TLTIU	rs,simm12
0c	TEQI	rs,simm12
0e	TNEI	rs,simm12
10	BLTZAL	rs,simm12
11	BGEZAL	rs,simm12
12	BLTZALL	rs,simm12
13	BGEZALL	rs,simm12

FIG. 6B

124

107 FUNC.	100 INSTRUCTION	102 OPERANDS
00	SLL	rd,rt,imm5
02	SRL	rd,rt,imm5
03	SRA	rd,rt,imm5
04	SLLV	rd,rt,rs
06	SRLV	rd,rt,rs
07	SRAV	rd,rt,rs
08	JR	rs
09	JALR	rd,rs
0c	SYSCALL	imm15
0d	BREAK	imm15
0f	SYNC	
10	MFHI	rd
11	MTHI	rs
12	MFLO	rd
13	MTLO	rs
18	MULT	rs,rt
19	MULTU	rs,rt,
1a	DIV	rs,rt
1b	DIVU	rs,rt

FIG. 6C

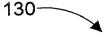
126

107 FUNC.	100 INSTRUCTION	102 OPERANDS
20	ADD	rd,rs,rt
21	ADDU	rd,rs,rt
22	SUB	rd,rs,rt
23	SUBU	rd,rs,rt
24	AND	rd,rs,rt
25	OR	rd,rs,rt
26	XOR	rd,rs,rt
27	NOR	rd,rs,rt
2a	SLT	rd,rs,rt
2b	SLTU	rd,rs,rt
30	TGE	rs,rt
31	TGEU	rs,rt
32	TLT	rs,rt
33	TLTU	rs,rt
34	TEQ	rs,rt
36	TNE	rs,rt

FIG. 6D

105 RS,RT.	100 INSTRUCTION	102 OPERANDS
00,*	MFC0	rt,rd
02,*	CFC0	rt,rd
04,*	MTC0	rt,rd
06,*	CTC0	rt,rd
08,00	BC0F	imm6
08,01	BC0T	imm6
08,02	BC0FL	imm6
08,03	BC0TL	imm6
1x,*	COP0	Func.(Fig.6F)

FIG. 6E



107 FUNC.	100 INSTRUCTION
01	TLBR
02	TLBWI
06	TLBWR
08	TLBP
10	RFE
18	ERET

FIG. 6F

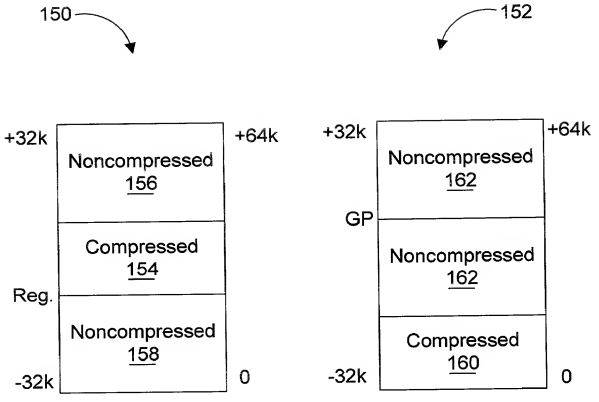

150
152
+32k
+64k
Noncompressed
156
Compressed
154
Reg.
Noncompressed
158
-32k
0
+32k
+64k
Noncompressed
162
GP
Noncompressed
162
Compressed
160
-32k
0

FIG. 7

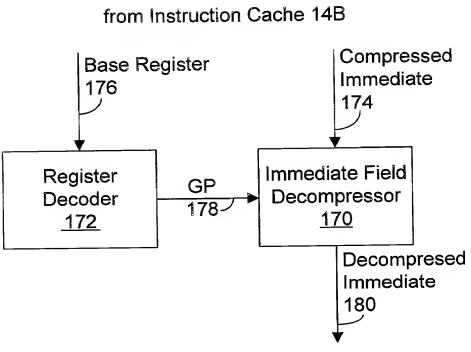

from Instruction Cache 14B
Base Register
176
Compressed
Immediate
174
Register
Decoder
172
GP
178
Immediate Field
Decompressor
170
Decompressed
Immediate
180

FIG. 8

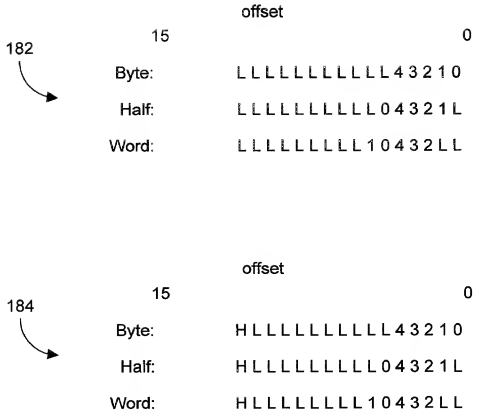

offset
15
0
182
Byte:
L L L L L L L L L L L 4 3 2 1 0
Half:
L L L L L L L L L L 0 4 3 2 1 L
Word:
L L L L L L L L L 1 0 4 3 2 L L
offset
15
0
184
Byte:
H L L L L L L L L L L 4 3 2 1 0
Half:
H L L L L L L L L L 0 4 3 2 1 L
Word:
H L L L L L L L L 1 0 4 3 2 L L

FIG. 9

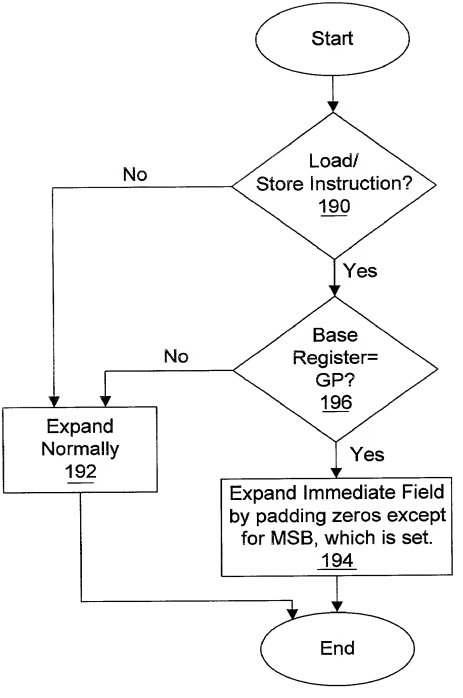

Start
Load/
Store Instruction?
190
No
Yes
Base
Register=
GP?
196
No
Yes
Expand
Normally
192
Expand Immediate Field
by padding zeros except
for MSB, which is set.
194
End

FIG. 10

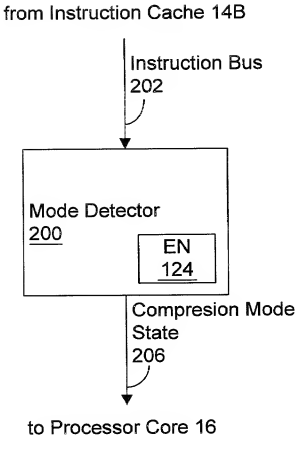

from Instruction Cache 14B
Instruction Bus
202
Mode Detector
200
EN
124
Compresion Mode
State
206
to Processor Core 16

FIG. 11

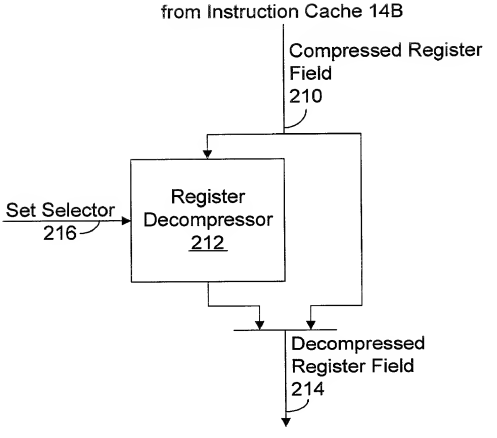

from Instruction Cache 14B
Compressed Register Field 210
Set Selector 216
Register Decompressor 212
Decompressed Register Field 214

FIG. 12

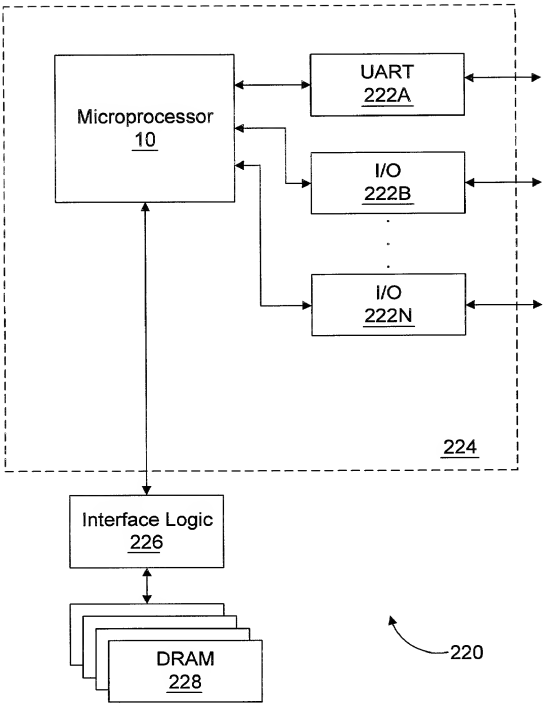

Microprocessor
10
UART
222A
I/O
222B
I/O
222N
224
Interface Logic
226
DRAM
228
220

FIG. 13